(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 October 2001 (04.10.2001)

PCT

(10) International Publication Number
WO 01/73741 A1

(51) International Patent Classification[7]: G09G 3/36

(21) International Application Number: PCT/EP01/02918

(22) International Filing Date: 15 March 2001 (15.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/537,825 29 March 2000 (29.03.2000) US

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: ALBU, Lucian, R.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). JANSSEN, Peter; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: BAELE, Ingrid, A., F., M.; Internationaal Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).

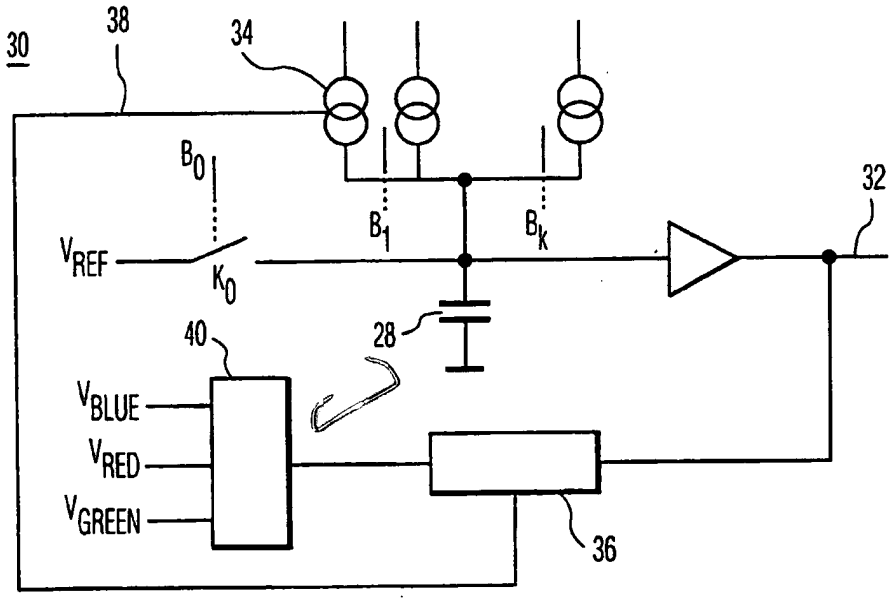
(81) Designated States *(national)*: JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DIGITALLY CONTROLLED CURRENT INTEGRATOR FOR REFLECTIVE LIQUID CRYSTAL DISPLAYS



(57) Abstract: A system for generating an image in an RLCD using current sources instead of voltage sources to reduce noise and power consumption. The current is provided by a plurality of RAM-driven IDACs. Each IDAC drives one of a plurality of RLCD columns in conjunction with one of a plurality of OTAs. A Look-Up-Table in each RAM holds a plurality of 6-bit digital values that correspond to the time-derivative of the values contained in gamma correction curves. The LUT values are automatically corrected at the end of each display cycle by an auto-correction.

WO 01/73741 A1

Digitally controlled current integrator for reflective liquid crystal displays

The invention relates to an image processing system for a reflective LCD.

The invention further relates to a reflective-LCD.

The invention further relates to a method for generating an image in a reflective-LCD.

In an RLCD having a matrix of m horizontal rows and n vertical columns, each m-n intersection forms a cell or picture element (pixel). By applying an electric potential difference, e.g., voltage, across a cell, a phase change occurs in the crystalline structure at the cell site and causes the pixel to change the incident light polarization vector orientation, thereby blocking the light from emerging from the electro-optical system. Removing the voltage across the pixel causes the liquid crystal in the pixel structure to return to the initial "bright" state. Variations in the applied voltage level produce a plurality of different gray shades between the light and dark limits.

Since an RLCD panel presents essentially a capacitive load to any drive circuit, a pulsed voltage ramp is typically employed to avoid high current spikes that are associated with driving such a capacitive load. At the individual columns is a comparator and a track-and-hold gating switch for terminating the individual column voltage rise when the column capacitance has charged to the predetermined voltage level needed to produce a particular grayscale, with each column terminating at a unique level along the global voltage ramp, thus producing a separate pulse-length modulating signal for each individual column.

At the end of a predetermined row time interval, the column charges stored in the intrinsic column capacitances are discharged to a reference voltage and the procedure is repeated for the next row. This process is repeated for all the m rows of the LCD to complete a single frame. Repetition of the frame activity allows for the continual updating of the displayed information. To better appreciate the above process, it would be beneficial to review U.S. Patent 4,766,430 to Gillette, et al, which is herein incorporated by reference.

Further, a non-linear gamma correction signal that is required to generate a required color distribution over the entire panel is superimposed on the ramped voltage

waveform. This gamma correction typically requires a digital bit resolution of 8 bits which when combined with the voltage ramp data produces a requirement for 13 bit resolution data words for the ramp signal generator. The principal drawback such an implementation is that such high bit resolution is difficult to integrate and dissipates higher power than a lower resolution solution.

An equally significant drawback of this prior art, however, is the noise associated with the voltage switching of the capacitive load of the LCD and the termination of the individual column charging by means of a gate. This noise capacitively couples into adjacent pixels and interferes with the display of accurate pixel data.

It is an object of the invention to provide an image processing system for a reflective-LCD which would lower the resolution requirements of drive circuitry in addition to reducing instantaneous columns switching currents and associated cross-talk interference.

This object is achieved with the image processing system in accordance with the invention as is specified in claim 1.

The image processing system generates an image in an RLCD from an Integrating Digital-to-Analog Converter (IDAC) having a current pulse output rather than a voltage pulse output. The current pulse output is integrated and filtered by the intrinsic capacitance of an RLCD panel column to reduce noise in and power consumption by the RLCD.

This IDAC is driven by a Look-Up-Table (LUT) within a Random Access Memory (RAM) used to store six bit time-derivative digital values of a non-linear gamma correction curve. These digital values are continually adjusted by an auto-correction module based on comparison between the resultant integrated column voltage and a fixed reference voltage for each color.

Further advantageous embodiments of the invention are specified in the dependent claims.

It is a further object of the invention to provide a reflective-LCD which would lower the resolution requirements of drive circuitry in addition to reducing instantaneous columns switching currents and associated cross-talk interference.

This object is achieved with the image processing system in accordance with the invention as is specified in claim 1.

It is a further object of the invention to provide a method for generating an image in a reflective-LCD.

This object is achieved with the method for generating an image in a reflective-LCD in accordance with the invention as is specified in claim 17.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawing:

Figure 1 shows a control circuit for generating the analog voltage excitation of the prior art,

Figure 2 shows a preferred embodiment of an analog current excitation path of an RLCD column with an auto-correction feedback loop according to the present invention,

Figure 3 shows a representative curve of gamma corrected brightness vs. voltage (BV) for a color RLCD and

Figure 4 shows typical waveforms generated for driving a color RLCD according to the present invention.

Figure 1 shows a control circuit 10 for generating the analog voltage excitation of the prior art. Since the present invention incorporates certain elements of circuit 10, a detailed review of its operation will aid in understanding the teachings of the present invention.

The analog excitation voltage comprises a timed series of small steps of voltage that are digitally generated beginning with counter 12 which is triggered by a precision clocking means (not shown). The output of counter 12, which has 256 sequential digital values in this example, provides addresses for a Look-Up-Table (LUT) in Random Access Memory (RAM) 14 at which are stored a plurality of digital data values representing the predetermined steps of a column excitation voltage waveform. Each digital data value has a resolution of 13 bits (8192 possible values). These digital data values are sequentially provided to the input of a digital-to-analog converter (DAC) 16 which transforms them into discrete steps of analog voltage that are presented to a group of column drivers 18.

This controlled excitation voltage provides the charging source for one or more of a plurality of columns 20 of the RLCD. In this example, 640 columns are supplied by a single waveform driver.

When a column voltage rises to the predetermined values provided in the data buffer 22, a comparator 24 for each column will cause the output of a column gate 26 to turn off, thereby halting the charge current to each column capacitance 28. The pixel is then displayed for the remainder of the row time interval. Other columns will continue to charge until their unique predetermined values are reached, at which time they will be turned off and the pixels displayed for the remainder of the row time.

At the end of the charge and display time, a "flight back" mode is entered whereby a high current switching device will quickly discharge the column capacitance back to a predetermined reference level within approximately 50 nanoseconds. The currents in this device can approach two amperes during this discharge operation. A representative RLCD device would have a structure of 1280 columns and 1024 rows and having an on-panel integrated pixel switch located between a pixel capacitance and a column, said switch being controlled by a row voltage signal.

Figure 2 shows a preferred embodiment of an analog current excitation circuit 30 using a monotonic current multiplier integrator with auto-correction according the present invention. The circuitry for background timing control and LUT digital value generation is identical to circuit 10, with the exception of: 1) DAC 16 is replaced with a plurality of integrating DACs (IDACs) having a current output; 2) RAM 14 is replaced with a plurality of RAM devices having a bit-resolution of at most eight bits; and 3) each one of the plurality of column gates 26 is replaced with an operational transconductance amplifier (OTA) at each column to switch the individual column currents.

In addition, separate ones of the aforementioned plurality of RAM and IDACs of the present invention are associated exclusively with a single column 20 of the RLCD. Furthermore, due to the integrating characteristic of the IDAC, digital voltage values within the LUT of circuit 10 are replaced by time-derivative values of currents required to produce gamma correction. Therefore, output voltage 32 follows the shape of the gamma correction curve as a result of column capacitance 28 being charged by the integrated analog excitation current produced by the aforementioned control elements, which in combination are represented symbolically as current source 34 in Figure 2.

At the end of each row time, auto-correction circuit 36 creates a corrected set of digital values 38 by comparing the peak value of output voltage 32 with the output of

multiplexer 40, which sequentially gates the maximum voltage levels of the three color reference voltages depending on the color of the pixel. These corrected values 38 are then loaded into the unique LUT for that column 20 to control current source 34 during the next integration cycle.

Figure 3 shows a representative BV curve of a color RLCD. In figure 3 a first curve 60 represents a voltage-brightness characteristic of the red pixels, a second curve 62 represents a voltage-brightness characteristic of the green pixels and a third curve 64 represents a voltage brightness characteristic of the blue pixels. These curves allows the IDAC resolution to be derived by determining a minimum voltage step ΔVmin that produces a change of one step (out of 256) to the brightness of the RLCD. Thus, the resolution required for a DAC is provided by the equation

$$N_{dac} = \left\{ \log_2 \frac{V\max - V\min}{\Delta V\min} \right\} + 1 = 11\,bits \qquad (1)$$

Since an IDAC performs a constant current integration with respect to time, the voltage at the IDAC output is linearly increasing with a slope proportional to the sum of the currents applied to the panel capacitance node, according to the equation

$$\Delta V_{idac} = \Delta t \frac{I}{C_{col}} \qquad (2)$$

where I is the current through C_{col}, and Δt is the integration time, during which I is retained at a constant value.

Thus, the resolution required by the IDAC is the minimum number of bits needed to generate said current and is governed by equation (1), wherein the maximum and minimum voltage steps on the BV curve create a one step brightness change in the RLCD. This resolution is described by the equation

$$N_{idac} = \left\{ \log_2 \frac{\Delta V\max}{\Delta V\min} \right\} + 1 = 6\,bits \qquad (3)$$

This reduced resolution of the IDAC provides for reduced integration complexity and power dissipation.

Since the IDAC generates binary weighted currents, the LUT stored values are calculated from the relationship between the BV values of Figure 3 and the column capacitance of the RLCD according to the equation

$$Vout(t) = \int_0^t \frac{I_{idac}(t)_{dt}}{C_{col}} - V_{ref} \qquad (4)$$

with $$I_{idac}(t)=\sum^{7} 2^k\, b_k\,(t) I_o \qquad (5)$$

where V_{ref} is the initial voltage setting at the start of the ramp, I_0 is the constant reference current, and $b_k(t)$ represents the binary coefficients for the input data word for k=0. . .7.

Further, for a given gamma correction data set Γ_k, where k=0. . .255, the system of equations which solve the values of $b_k(t)$ is provided by the equation

$$\left|\Gamma_k - \frac{I_o}{C_{col}}\tau \sum_{j=0}^{k}\sum_{m=0}^{7} 2^m\, b_m\,(j)\right| \le \epsilon \qquad (6)$$

with τ representing the integration time (clock period) between two adjacent samples and ϵ being the acceptable error which must be less than the minimum voltage corresponding to a single gray level on the RLCD.

Thus, the system provides a unique solution for gamma correction curves which are monotonic and belong to a polynomial ring, said polynomial providing for mapping to a system LUT of 256 values of 8 bits, such lower resolution data values providing for reduced integration area and reduced power dissipation.

Figure 4 shows typical waveforms generated for driving a color RLCD according to the present invention. The low controlled current provided by the transconductance current source of the present invention is integrated by the panel capacitance to produce a controlled voltage rise on the columns and avoids the generation of the noisy instantaneous spikes of current.

Waveform 42 represents a typical ramped resultant voltage waveform during the row period. Waveform 44 shows the first latching signal applied to the charging OTA, and Waveform 46 illustrates the resulting envelope of an individual column voltage that results from Waveform 44. While waveform 46 implies a constant amplitude current pulse, the actual waveshape of the charging current applied can be of any of a plurality of waveshapes and is exclusively controlled by the LUT within RAM 14. Auto-correction occurs at time 48 and column discharge is a time 50.

Numerous modifications to the alternative embodiments of the present invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. Details of the structure may be varied substantially without departing from the spirit of the invention and the exclusive use of all modifications which come within the scope of the claims is reserved.

CLAIMS:

1. An image processing system for an reflective LCD, comprising:

a digital data generating means for providing digital values to one or more of a plurality of ,

a plurality of integrating Digital-to-analog Converter which provide analog current outputs in response to said digital values;

an reflective LCD device comprised of a plurality of vertical columns (20) and a plurality of horizontal rows;

a reflective LCD column selection means;

a reflective LCD row selection means;

a discharge means for returning the voltage on each one of a plurality of columns (20) to a reference voltage at the end of a row time; and

an auto-correction means (36) for implementing gamma correction of the analog current outputs.

2. The image processing system according to claim 1, wherein the digital data generating means comprises:

a digital counter (12) for providing addresses to a random access memory (14); and

a random access memory (14) having a look-up table for storing a plurality of time-derived digital values corresponding to a different one of a plurality of gamma brightness levels in the reflective LCD.

3. The image processing system according to claim 2, wherein the look-up table is comprised of 256 digital values having at most a binary word length of 8 bits each.

4. The image processing system according to claim 2, wherein the look-up table values are changed dynamically in response to a correction signal (38) generated by the auto-correction means (36).

5. The image processing system according to claim 2, wherein the digital values stored in the look-up table, $b_m(j)$, are derived using the equation

$$\left|\Gamma_k - \frac{I_o}{C_{col}} \tau \sum_{j=0}^{k} \sum_{m=0}^{7} 2^m b_m(j)\right| \leq \epsilon$$

6. The image processing system according to claim 2, wherein the image processing system includes a plurality of integrated Digital-to-analog Converter and random access memory (14), wherein each column (20) of the reflective LCD is associated with a separate one of the plurality of integrated Digital-to-analog Converter and random access memory (14).

7. The image processing system according to claim 1, wherein the column selection means is comprised of a plurality of operational transconductance amplifiers, wherein each separate one of the plurality of operational transconductance amplifiers is connected in series with a separate one of the plurality of columns (20).

8. The image processing system according to claim 7, whereby operational transconductance amplifier conduction begins at the start of a row time period and ends in response to a latching input signal that is generated as a result of a digital comparison between a stored data value corresponding to a desired pixel voltage for a particular one of the plurality of columns (20) and a digital counter (12) output value.

9. The image processing system according to claim 1, wherein the discharge means is a MOS switch.

10. An auto-correction system for an reflective LCD, comprising:
a multiplexer (40) for presenting a plurality of reference color voltages to a correction circuit (36);
a sensor for detecting the output voltage level (32) of the reflective LCD;
an analog comparator for determining the relative voltages of the output voltage (32) of the reflective LCD and the reference color voltage; and
a correction means (36) for providing control signals (38) to an input of one of a plurality of digital data generating means for use in a next excitation cycle.

11. The auto-correction system for an reflective LCD according to claim 10, wherein the correction means (36) causes the loading of new digital derivative values to the, said values corresponding to those values required to correct the column voltage rise based on a gamma correction relationship to the applied column voltage, said values to be used for waveform generation during the next cycle.

12. The auto-correction system for an reflective LCD according to claim 10, wherein look-up table values are derived using the equation

$$\left| \Gamma_k - \frac{I_o}{C_{col}} \tau \sum_{j=0}^{k} \sum_{m=0}^{7} 2^m b_m(j) \right| \leq \epsilon$$

13. An reflective LCD device, comprising:
a row switch integrated at each different one of a plurality of pixel locations;
a matrix structure comprised of a plurality of vertical columns (20) and a plurality of horizontal rows;
a plurality of random access memory (14) and a plurality of integrating Digital-to-analog Converters, wherein separate ones of the plurality of random access memory (14) and the plurality of integrating Digital-to-analog Converters are associated with each different one of the plurality of vertical columns (20); and
a column selection means for beginning and ending current flow to each different one of a plurality of columns in response to a logical input signal.

14. The reflective LCD device according to claim 13, wherein the matrix structure is comprised of 1280 columns (20) and 1024 rows.

15. The reflective LCD device according to claim 13, wherein the random access memory (14) for each different one of a plurality of columns (20) holds the derivative digital values required for gamma correction of the output current to that column.

16. The reflective LCD device according to claim 13, wherein each different one of a plurality of integrating Digital-to-analog Converters provides a current output.

17. The reflective LCD device according to claim 13, wherein the column selection means comprises an operational transconductance amplifier.

18. A method for generating an image in an reflective LCD, comprising the steps of:

a) sequentially obtaining a first one of a plurality of digital values within a look-up table;

b) time-integrating the digital value;

c) converting the time-integrated digital value to an analog current value;

d) time-integrating the analog current value;

e) repeating steps a-d for each other one of the plurality of digital values within the look-up table until a predetermined terminating digital value is attained; and

d) comparing the highest analog voltage level attained by any one of the plurality of columns (20) to a reference voltage for correcting the digital values within the look-up table.

19. The method according to claim 18, wherein the plurality of digital values stored within the look-up table are the time-derivative of the plurality of current values required to create gamma brightness correction when integrated with the intrinsic column capacitance (28) of the reflective LCD.

20. The method according to claim 19, wherein the digital values contained within the look-up table $b_m(j)$ are derived using the equation

$$\left| \Gamma_k - \frac{I_o}{C_{col}} \tau \sum_{j=0}^{k} \sum_{m=0}^{7} 2^m b_m(j) \right| \leq \epsilon$$

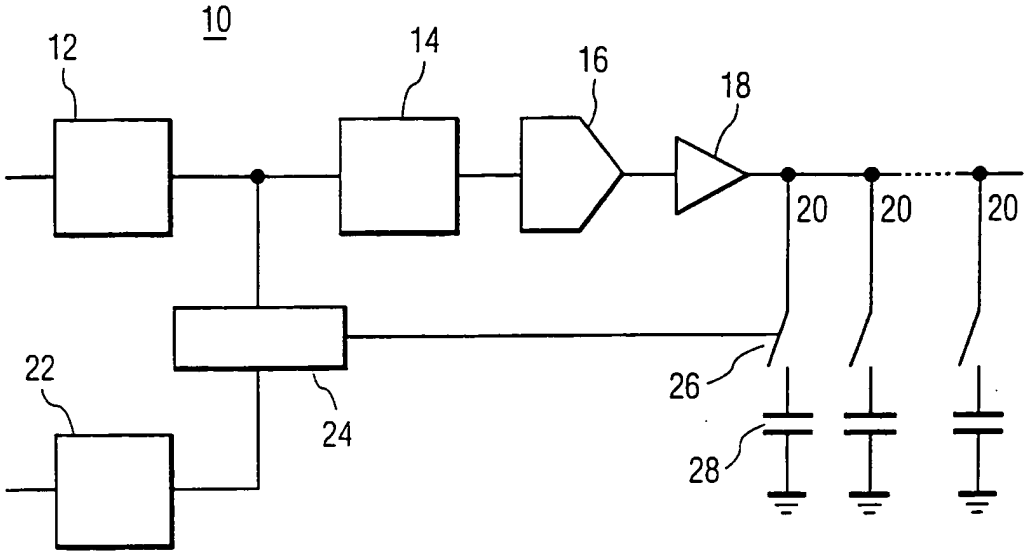

10
12
14
16
18
20
20
20
22
24
26
28

FIG. 1

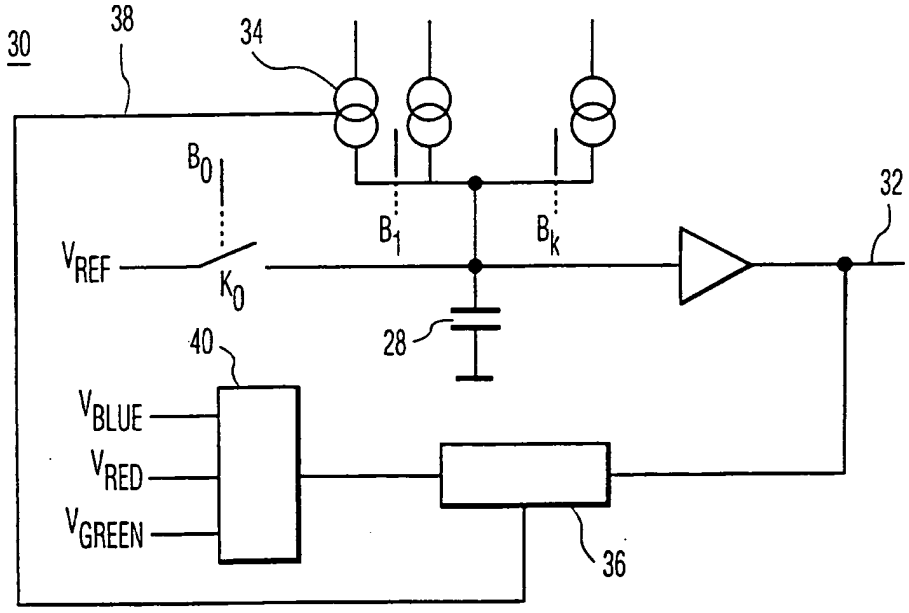

30
38
34
B_0
B_1
B_k
32
V_{REF}
K_0
28
40
V_{BLUE}
V_{RED}
V_{GREEN}
36

FIG. 2

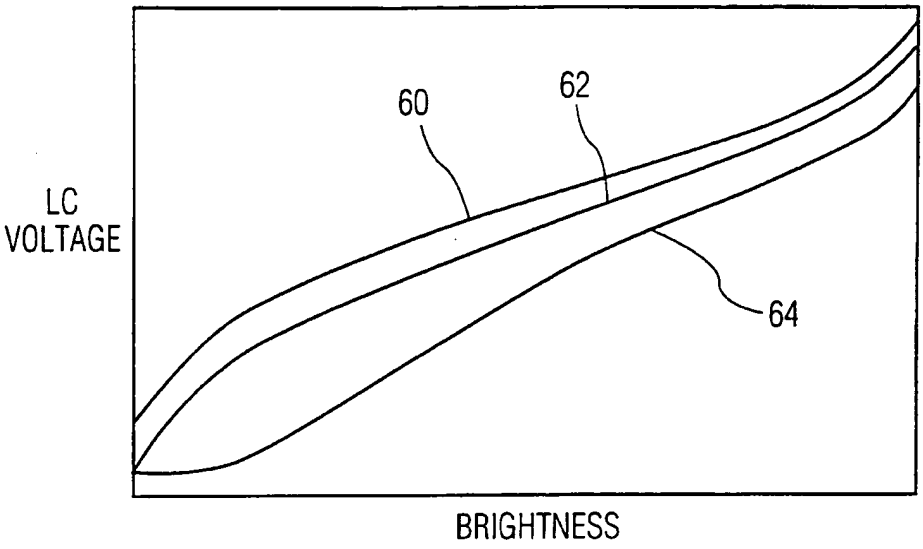


FIG. 3

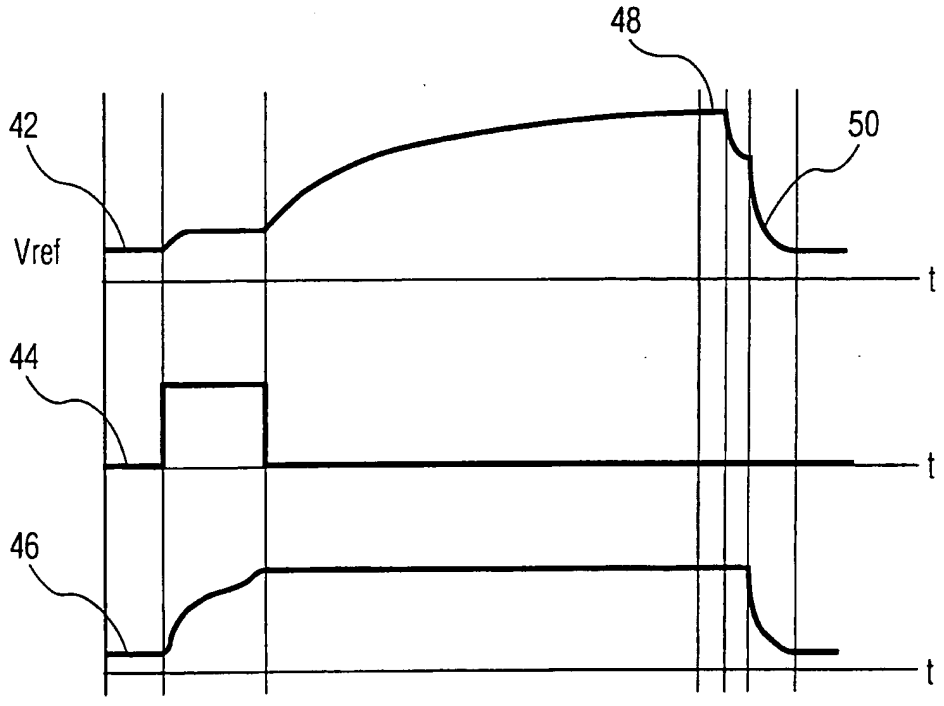


FIG. 4

INTERNATIONAL SEARCH REPORT

In' ·ational Application No
PCT/EP 01/02918

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 724 036 A (SAKAGUCHI YOSHITAMI ET AL) 3 March 1998 (1998-03-03) see abstract column 1, line 7 - line 9 column 1, line 32 - line 39 column 2, line 8 - line 28 column 3, line 60 -column 5, line 3; figure 1 --- -/--	1-3, 13-16, 18,19

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 August 2001	13/08/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Corsi, F

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 01/02918

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 648 791 A (TAKESHITA SHOICHI ET AL) 15 July 1997 (1997-07-15) see abstract column 1, line 12 -column 2, line 24; figure 20 column 2, line 52 - line 58 column 3, line 20 - line 51 column 4, line 52 -column 5, line 42; figure 1	1-3, 13-16, 18,19
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 11, 28 November 1997 (1997-11-28) -& JP 09 179530 A (FUJITSU LTD), 11 July 1997 (1997-07-11) abstract	1-3, 13-16, 18,19
A	EP 0 634 737 A (PHILIPS ELECTRONICS UK LTD ;PHILIPS ELECTRONICS NV (NL)) 18 January 1995 (1995-01-18) see abstract column 4, line 34 - line 54; figures 1,2 column 6, line 30 - line 49	10

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Ir ational Application No
PCT/EP 01/02918

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5724036 A	03-03-1998	JP 2708380 B	04-02-1998
		JP 8084307 A	26-03-1996
US 5648791 A	15-07-1997	US 5453757 A	26-09-1995
		DE 69214872 D	05-12-1996
		DE 69214872 T	13-03-1997
		EP 0510696 A	28-10-1992
		JP 2743683 B	22-04-1998
		JP 5094159 A	16-04-1993
		KR 9610729 B	07-08-1996
JP 09179530 A	11-07-1997	NONE	
EP 0634737 A	18-01-1995	DE 69410543 D	02-07-1998
		DE 69410543 T	24-12-1998
		JP 7079396 A	20-03-1995
		US 5459483 A	17-10-1995